WHAT IS CLAIMED IS:

1. A method of synchronizing a VCO clock with a serial data stream, comprising:

receiving a reference clock signal having a first frequency and a VCO clock signal having a second frequency, the VCO clock signal intended to be synchronized with a serial data stream;

generating a beat frequency related to a difference between the first frequency and the second frequency;

measuring an interval between at least a first beat and a second beat;

determining if the interval exceeds a first predetermined amount;

if the interval fails to exceed the first predetermined amount, indicating that the first frequency and the second frequency are not sufficiently matched, and synchronizing the VCO clock signal with the reference clock signal.

2. The method as defined in Claim 1, wherein the interval is measured using a counter synchronized with the reference clock to count a number of clocks between the first beat and the second beat.

3. The method as defined in Claim 1, wherein upon determining that the interval exceeds the first predetermined amount, indicating that the first frequency and the second frequency are sufficiently matched, and synchronizing the VCO clock signal with the serial data stream.

4. The method as defined in Claim 1, wherein the interval is selected based on a lock range of a phase locked loop.

5. A method of presetting a phase locked loop to a lock range of a bitstream receiver clock with a network bitstream, the method comprising:

generating a beat frequency from a reference clock and a bitstream receiver clock, wherein the reference clock has a reference clock frequency and the bitstream receiver clock has a receiver frequency;

based on the beat frequency, determining if the receiver clock frequency varies by more than a first predetermined amount from a frequency associated with the bitstream;

temporarily locking the receiver frequency to the reference clock frequency at least partly in response to determining that the receiver clock frequency varies by more than the first predetermined amount; and

synchronizing the receiver clock frequency to the bitstream at least partly in response to determining that the receiver clock frequency does not vary by more than the first predetermined amount.

6. The method as defined in Claim 5, wherein the first predetermined amount is selected at least in part based on a lock range of a phase locked loop used to synchronize the bitstream receiver clock with the bitstream.

7. The method as defined in Claim 5, wherein the act of determining if the receiver clock frequency varies by more than the first predetermined amount from the frequency associated with the bitstream further comprises measuring an interval between beats of the beat frequency.

8. The method as defined in Claim 5, further comprising:

clearing a first error bit at least partly in response to determining that the receiver clock frequency does not vary by more than the first predetermined amount; and

providing a warning signal at least partly in response to determining that the receiver clock frequency does vary by more than the first predetermined amount.

9. The method as defined in Claim 5, further comprising providing a warning signal at least partly in response to determining that the receiver clock frequency does vary by more than the first predetermined amount.

10. A method of preparing a VCO clock for synchronization with a bitstream, comprising:

receiving a reference clock signal having a first frequency and the VCO clock signal having a second frequency, the VCO clock signal intended to be synchronized with a serial data stream;

generating a beat frequency related to a difference between the first frequency and the second frequency;

measuring an interval between at least a first beat and a second beat;

determining if the interval exceeds a first predetermined amount; and

if the interval fails to exceed the first predetermined amount, which indicates that the first frequency and the second frequency are not sufficiently matched, synchronizing the VCO clock signal with the reference clock signal.

11. The method as defined in Claim 10, wherein the interval is measured using a counter synchronized with the reference clock to count a number of clocks between the first beat and the second beat.

12. The method as defined in Claim 10, wherein upon determining that the interval exceeds the first predetermined amount, which indicates that the first frequency and the second frequency are sufficiently matched, synchronizing the VCO clock signal with the serial data stream.

13. The method as defined in Claim 10, wherein the interval is selected based on a lock range of a phase locked loop circuit.

14. A synchronization acquisition circuit, comprising:

a first clock terminal configured to receive a first clock signal;

a second clock terminal configured to receive a second clock signal;

a differentiator circuit coupled to the first and the second clock terminals, the differentiator circuit configured to generate a beat signal having a beat frequency based on the first and second clock signals;

a beat interval circuit coupled to the differentiator circuit, the beat interval circuit configured to determine when a beat interval range of the beat signal exceeds a predetermined threshold, the beat interval circuit further configured to generate a signal that causes the first clock to be synchronized with the second clock when the threshold is not exceeded within a first period of time.

15. The synchronization acquisition circuit as defined in Claim 14, wherein the threshold is selected based on a lock range of a phase locked loop circuit.

16. The synchronization acquisition circuit as defined in Claim 14, further comprising an anti-falsing circuit coupled to the beat interval circuit, the anti-falsing circuit configured to prevent the beat interval circuit from generating the signal that

causes the first clock to be synchronized with the second clock unless a first condition is met.

17. The synchronization acquisition circuit as defined in Claim 14, wherein the differentiator circuit further comprises a first full wave differentiator circuit coupled to an in-phase clock signal derived from the first clock signal and a second full wave differentiator circuit coupled to a quadrature phase clock signal derived from the first clock signal.

18. The synchronization acquisition circuit as defined in Claim 14, wherein the first clock signal is output from a voltage controlled oscillator and the second clock signal is a reference clock signal.